

Lab Report - 04

Course No: 206

Course Title: Digital Logic Design

**Submitted To:**

Iffat Tamanna

Dept: CSE

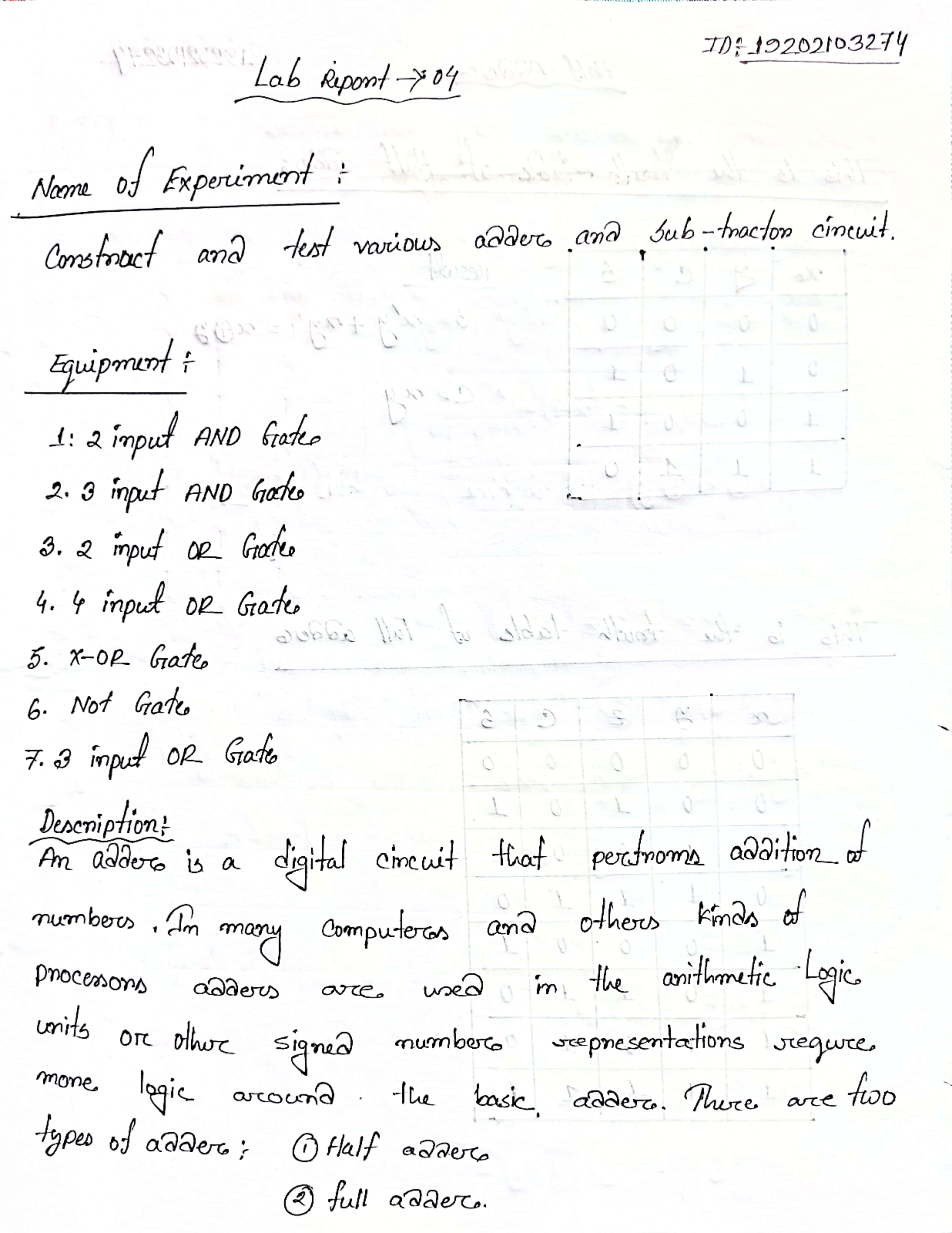
**Submitted By:**

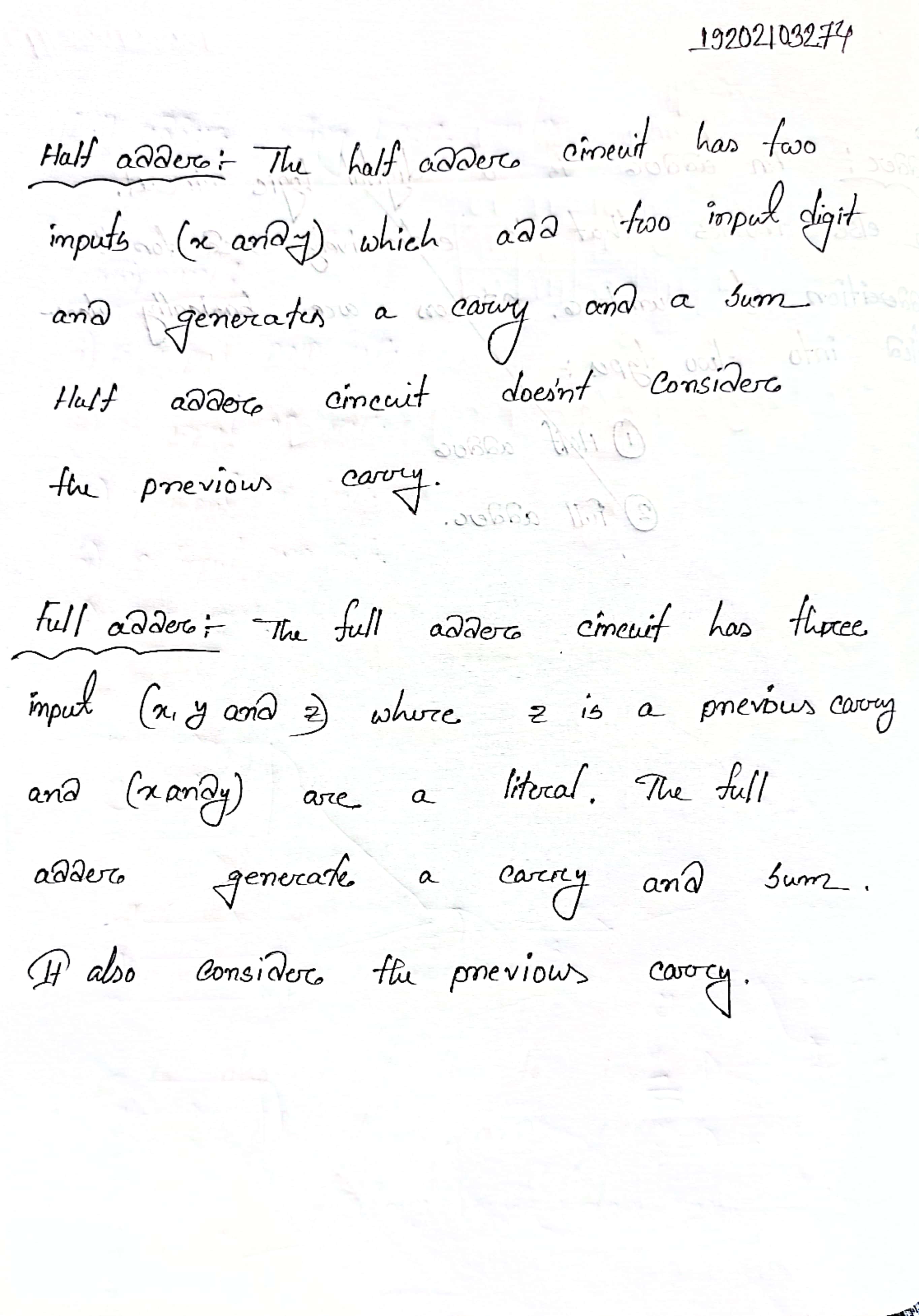
Md: Zobayer Hasan Nayem

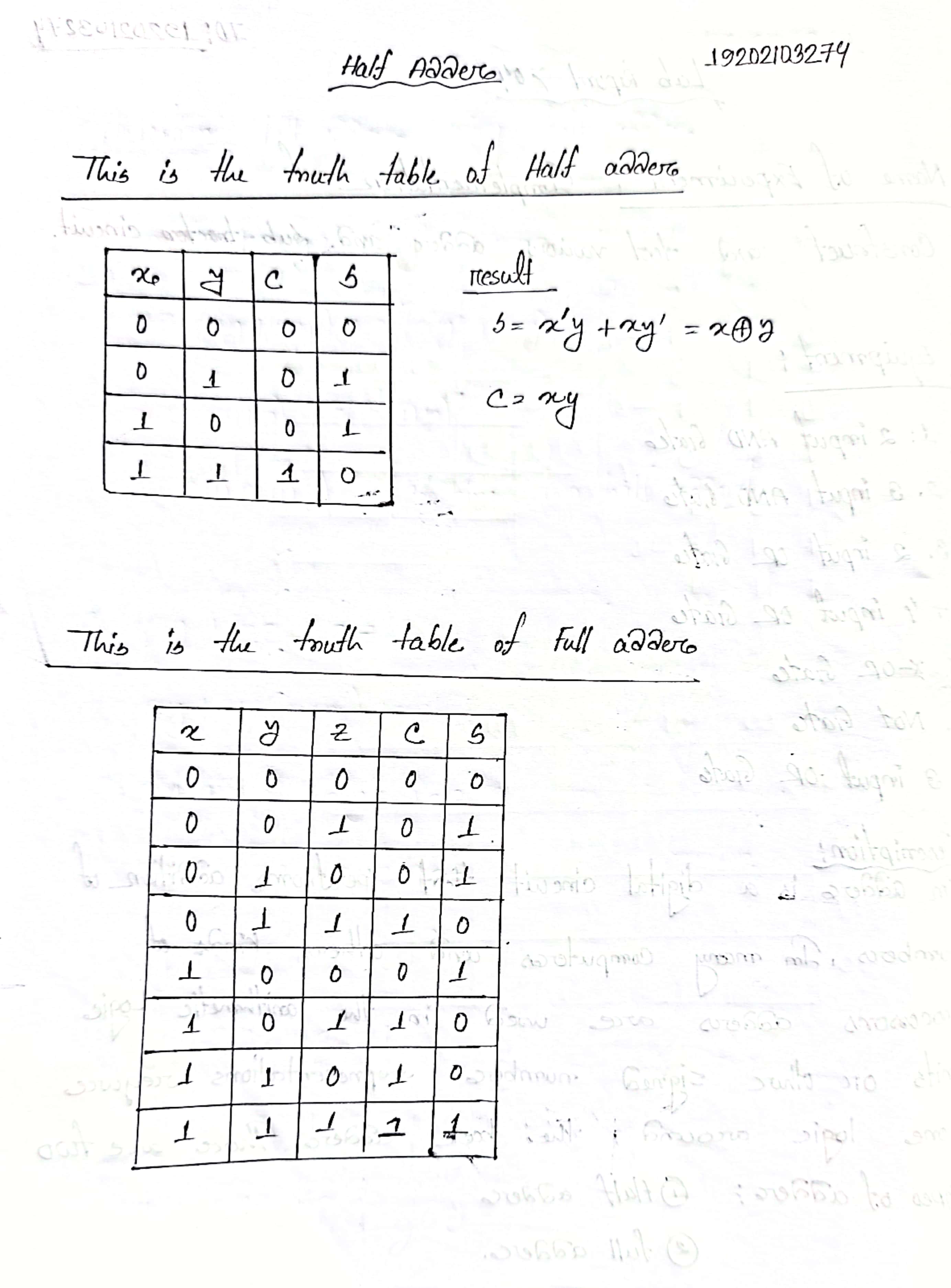
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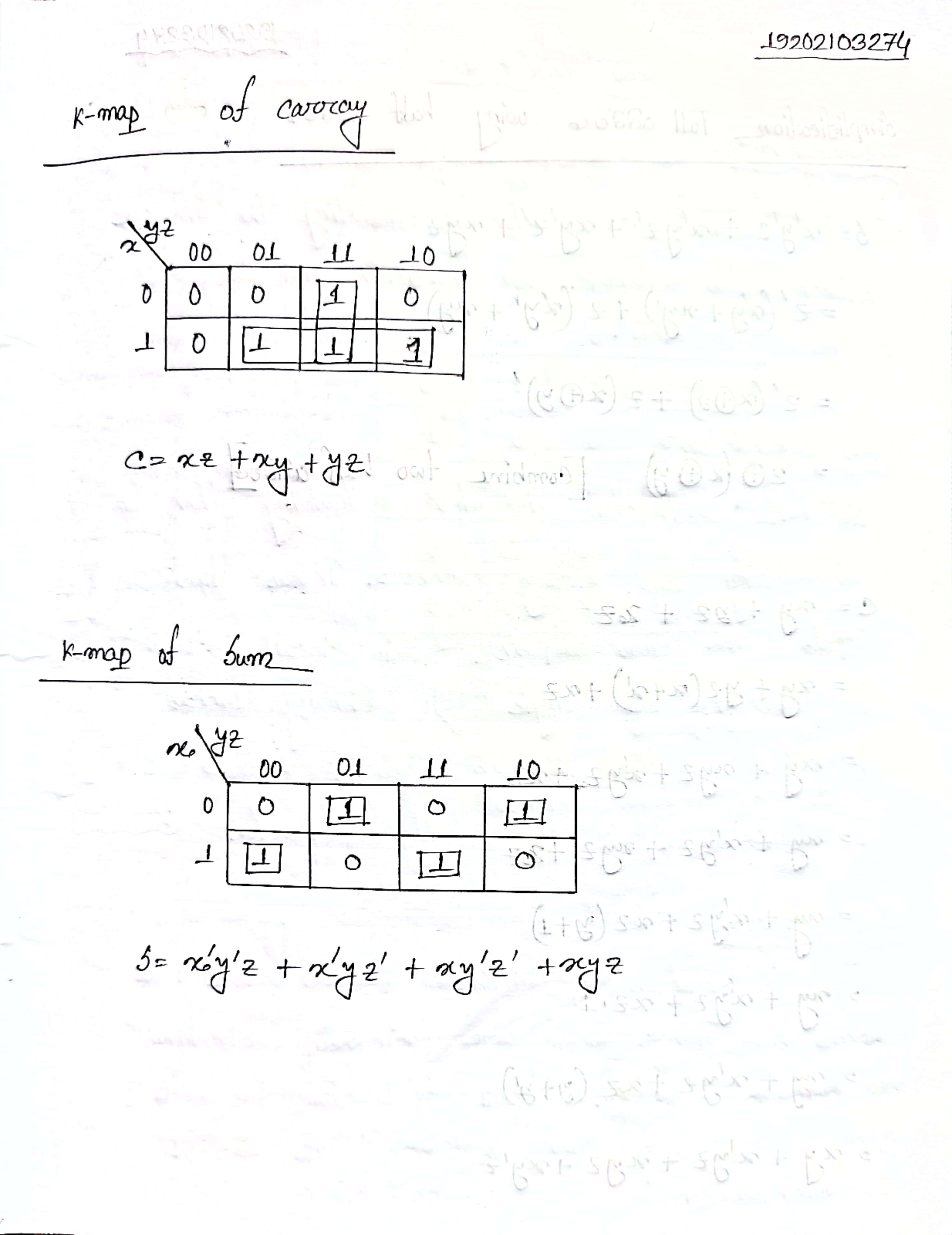
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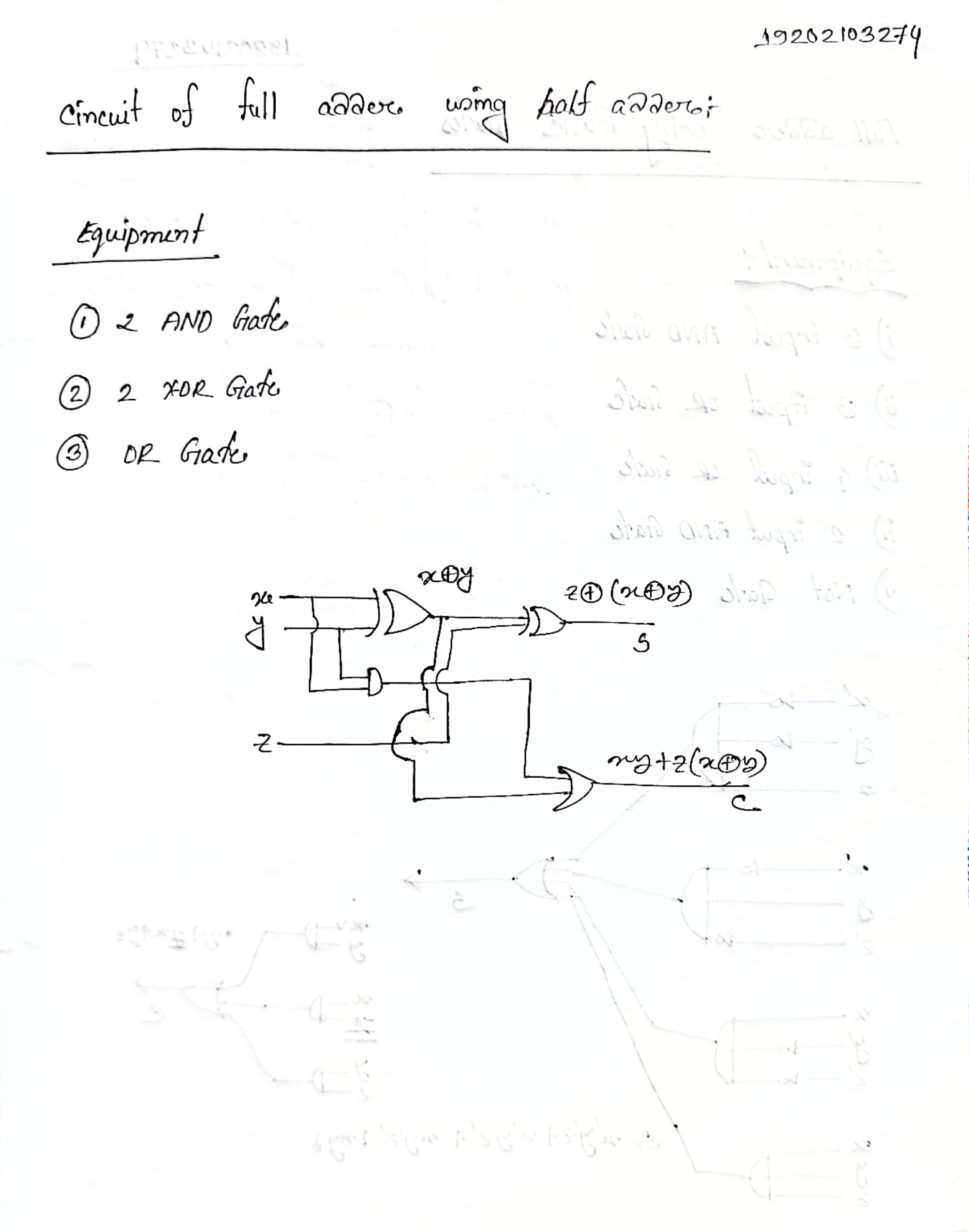
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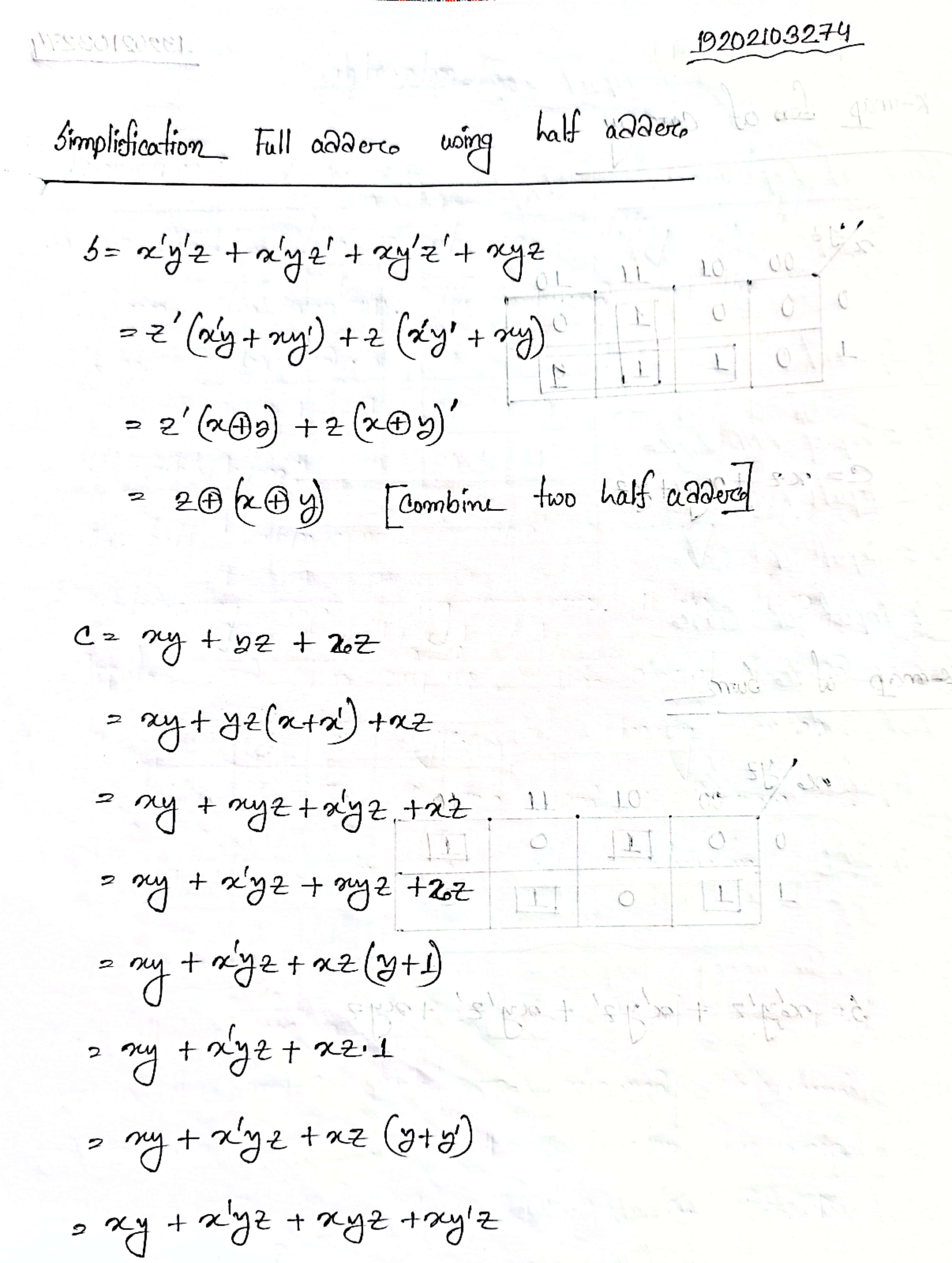


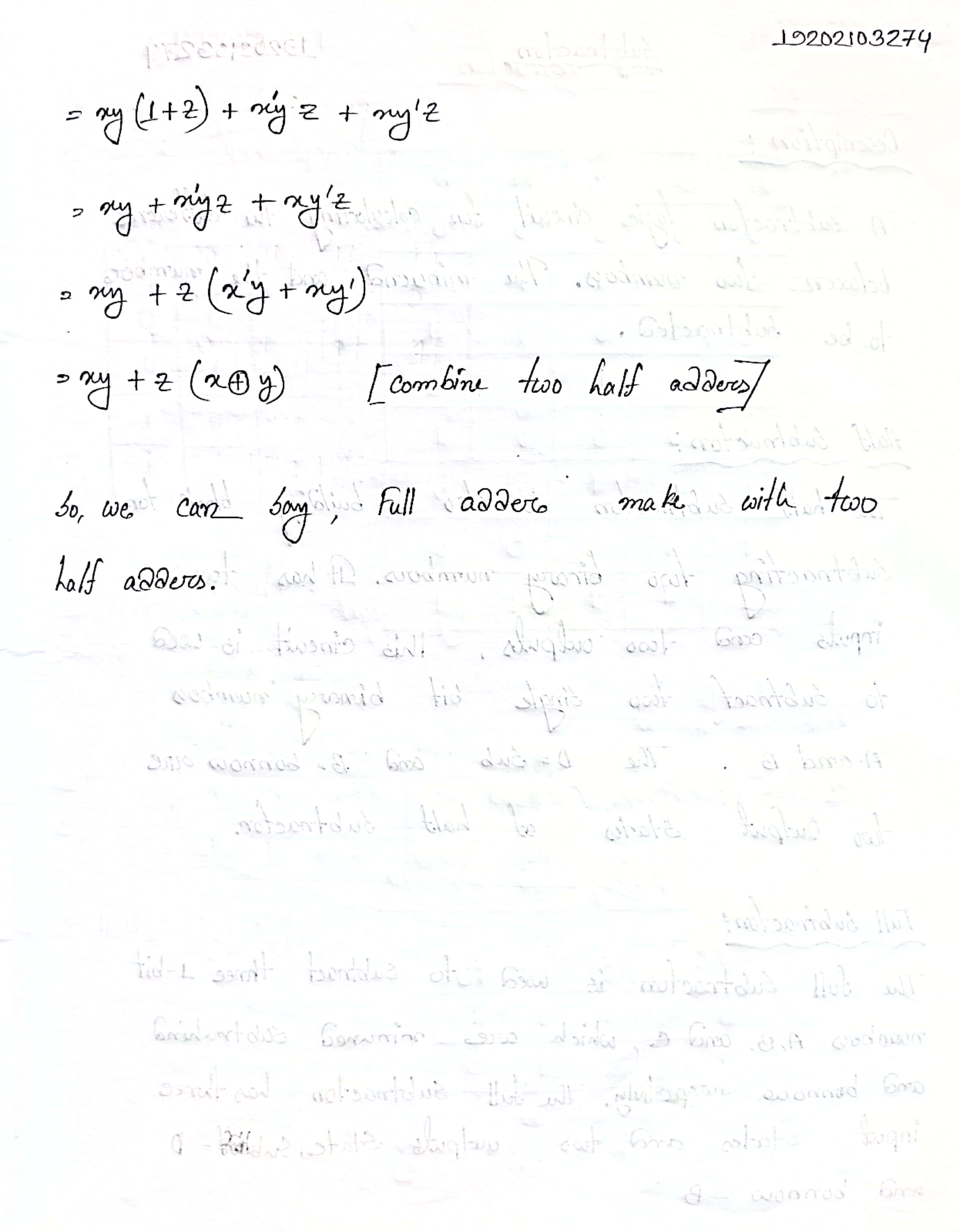


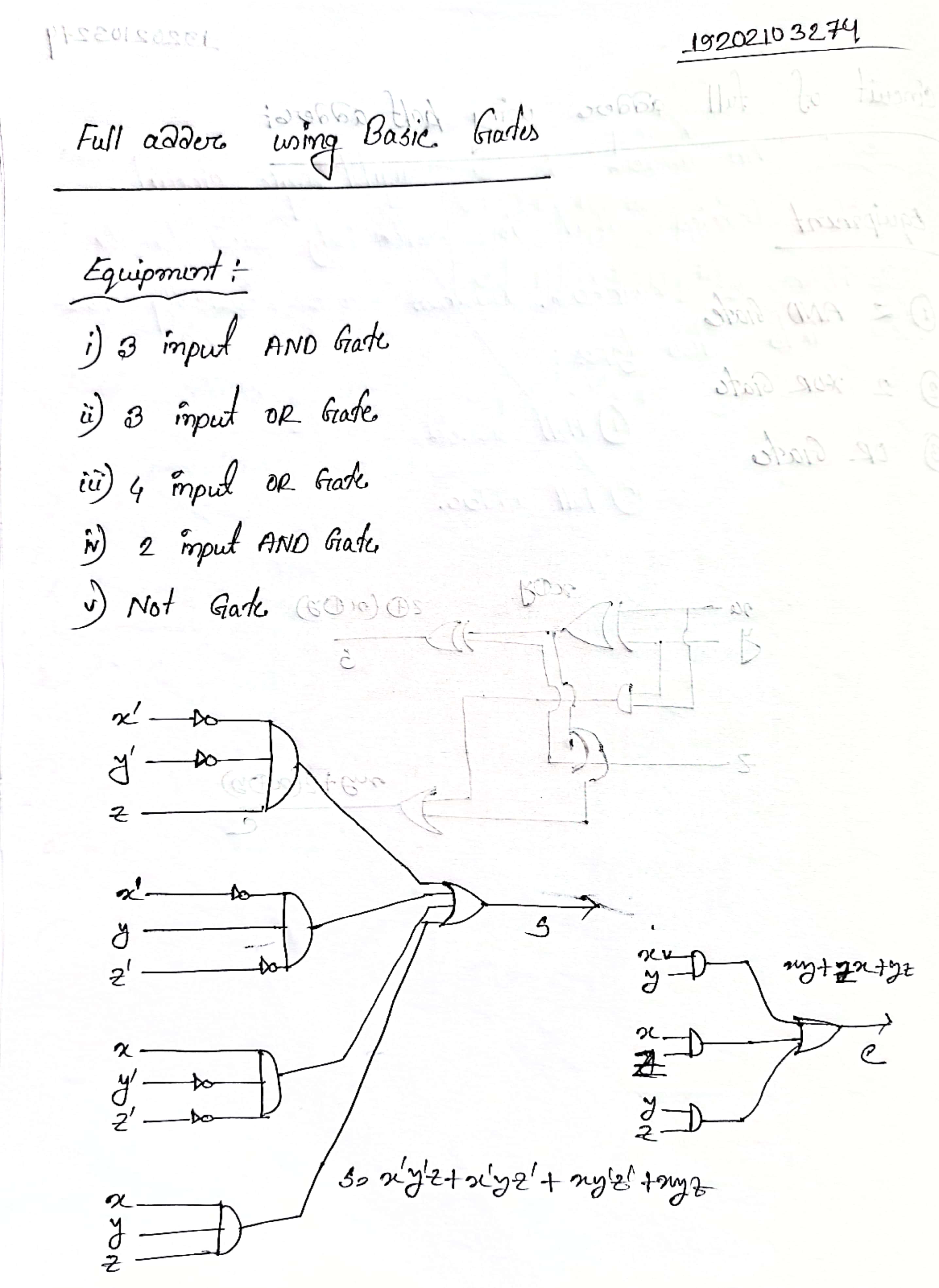


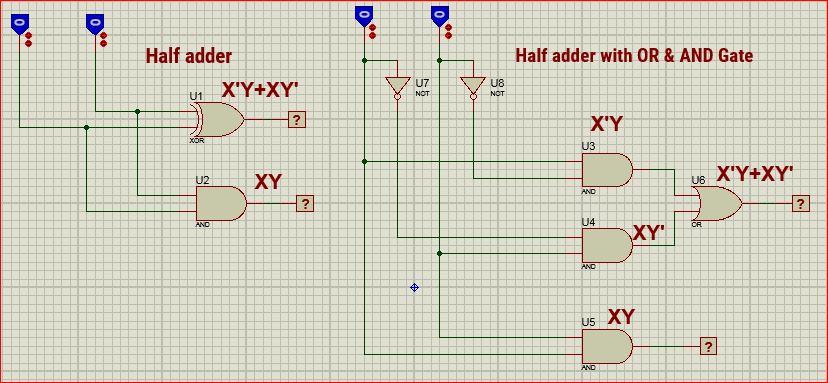


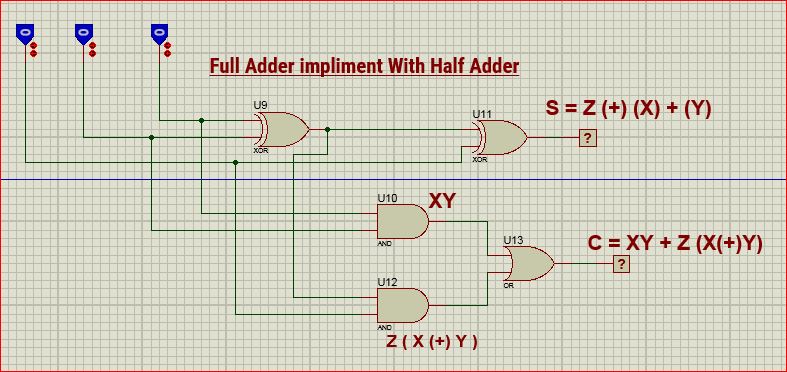


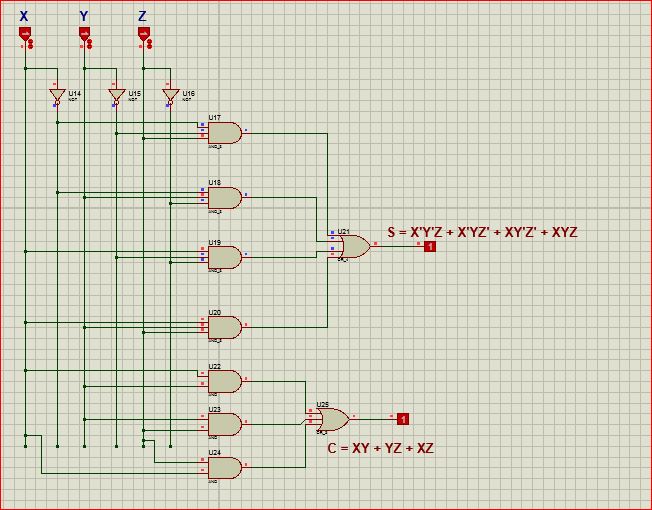












Full Adder Using Basic Gates

